ZKW AF

Docket No.: L&L-I0050

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MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: July 25, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/932,891 Confirmation No.:6815
Inventor	:	Jens Sauerbrey
Filed	:	August 20, 2001
Title	:	Variable Clock Configuration for Switched OP-AMP Circuits
TC/A.U.	:	2116
Examiner	:	Tse W. Chen
Customer No.	:	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated April 18, 2005, finally rejecting claims 1-5 and 7-31.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

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Real Party in Interest:

This application is assigned to INFINEON TECHNOLOGIES AG of Munich, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-5 and 7-31 are rejected and are under appeal. Claim 6 was cancelled in an amendment dated September 23, 2004.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was submitted on May 23, 2005. The Primary Examiner stated in an *Advisory Action* dated ** that the request for reconsideration had been considered but did not place the application in condition for allowance.

Summary of the Claimed Subject Matter:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to a circuit configuration in switched op-amp

technology and to a method for clocking successive operational amplifier stages constructed in switched op-amp technology.

Appellants explained on page 17 of the specification, line 2, that in all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case.

Appellants further explained on page 17 of the specification, line 6, that, referring now to the figures of the drawings in detail and first, particularly to FIG. 1 thereof, there is shown a prior art switched op-amp circuit that includes two operational amplifier stages. The operational amplifier 1, the sampling capacitor 2, the integration capacitor 3, and the capacitor 4 form the first operational amplifier stage. The second operational amplifier stage includes the operational amplifier 5, the sampling capacitor 6, the integration capacitor 7, and the capacitor 8. The various switches shown in FIG. 1 are switched on and off by two non-overlapping switching-clock signals that will be called even and odd switching-clock signals in the text that follows. Before discussing the operation of the circuit shown in FIG. 1 in greater detail, the generation of these two switching-clock signals will be explained with reference to FIGS. 2A and 2B.

Appellants outlined on page 17 of the specification, line 22, that, Fig. 2A illustrates a prior art clock generator for generating a non-overlapping two-phase clock. A rectangular input clock signal 21 having the frequency f_{clk} is applied to the input of the circuit. The variation with time of the input clock signal 21 is shown in FIG. 2B.

Appellants stated on page 18 of the specification, line 2, that the input clock signal 21 is present, on one hand, at the input of the inverter 22 and also at an input of the second NOR gate 24. The output of the inverter 22 is connected to an input of the first NOR gate 23. At the output of the NOR gate 23, the output signal 25 is present that is delayed by the two inverters 26. At the output of the inverter chain, the even switching-clock signal 27 can be picked up, the variation with time of which is shown in FIG. 2B. The even switching-clock signal 27 is connected to the second input of the second NOR gate 24, at the output of which the output signal 28 appears. The output signal 28 is delayed by the two inverters 29 and, at the output of the inverter chain, the odd switching-clock signal 30 can be picked up, the variation of time of which is also shown in FIG. 2B. The odd switching-clock signal 30 is supplied to the second input of the first NOR gate 23.

Appellants mentioned on page 18 of the specification, line 18, that the comparison of the variation of the even switching-clock signal 27 and of the odd switching-clock signal 30 by referring to FIG. 2B shows that the odd switching-clock signal 30 is in each case switched off during the on-phase of the even switching-clock signal 27. In addition, both switching-clock signals are in a common off-phase between the on-phase of the even switching-clock signal 27 and the on-phase of the odd switching-clock signal 30 during the period δ. It is, therefore, called a "non-overlapping two-phase clock".

Appellants described on page 19 of the specification, line 2, that each of the switches shown in FIG. 1 is now switched on and off by the even switching-clock signal or by the odd switching-clock signal. Next to each switch, the switching clock by which it is clocked is noted.

Appellants described on page 19 of the specification, line 7, that firstly, the first operational amplifier stage will now be considered during the on-phase of the even switching clock. The switches 9 and 10 are closed, therefore, whereas the switches 11, 12, 13 and 14 are open. The operational amplifier 1 is, therefore, inactive in such a phase. The input signal IN is present at one terminal of the sampling capacitor 2 and the other terminal is connected to VSS. The

sampling capacitor 2 is, therefore, charged up by the input signal. The capacitor 4 is connected to VSS and VDD through the switches 9 and 10 and is, therefore, charged up by the supply voltage. The on-phase of the even switching-clock signal is followed - after a short common off-phase of both switching-clock signals - by the on-phase of the odd switching-clock signal. During such a phase, the switches 9 and 10 are open whereas the switches 11, 12, 13 and 14 are closed. Therefore, the operational amplifier 1 is switched on in the phase. One terminal of the sampling capacitor 2 is connected to VDD through the switch 12. The other terminal of the capacitor 2 is connected to the inverting input of the operational amplifier 1 through the switch 13. The capacitor 4 that is connected to VSS through the switch 14 in the phase additionally couples in a constant charge that produces a type of DC shift. The injected charge makes it possible to achieve an approximate potential VSS at the inverting input. The operational amplifier 1, as the active component, now attempts to correct its output to such an extent that the difference between the input voltages becomes zero. Therefore, the operational amplifier 1 attempts to bring the inverting input to VSS potential. As a result, precisely the charge quantity that has been sampled at the sampling capacitor 2 is transferred to the integration capacitor 3.

As set forth on page 20 of the specification, line 13, the second operational amplifier stage is operated in the opposite phase to the first one. Still being considered is the on-phase of the odd switching clock in which the operational amplifier 1 is active. The switches 15 and 16 of the second op-amp stage are closed and that is why the output of the operational amplifier 1 charges up the sampling capacitor 6 belonging to the second operational amplifier stage. Thus, the integration-phase of the first operational amplifier stage and the sampling phase of the second operational amplifier stage are taking place at the same time.

Appellants further mentioned on page 20 of the specification, line24, that, in the subsequent switching-clock phase, the charge quantity sampled at the sampling capacitor 6 is transferred to the integration capacitor 7. During such integration-phase of the second operational amplifier stage, the first operational amplifier stage is already back in the sampling phase.

As stated on page 21 of the specification, line 4, the switching clock configuration shown in FIG. 2B is modified by the invention such that the on times of the operational amplifiers are shortened and, thus, a power saving is achieved. The hardware according to the invention is

illustrated in FIG. 3. A programmable clock generator 31 is supplied with a squarewave input clock signal 32 having the frequency f_{clk}. A circuit 33 for determining the transistor switching speed determines the switching speed of the transistors that is significant for the transient response of the operational amplifiers. A pulse signal 34 characteristic of the switching speed is supplied to the programmable clock generator 31 and taken into consideration in the generation of the even switching-clock signal 35 and of the odd switching-clock signal 36. The faster the switching of the devices are, the shorter the on-phases of the operational amplifiers can be.

As further explained on page 21 of the specification, line 21, FIG. 4 illustrates an example for a circuit 33 for determining the transistor switching speed. The input clock signal 37 is present at the first input of the XOR gate 40. At the second input of the XOR gate 40, the delayed and inverted clock signal 39 is present that is obtained from the input clock signal 37 by an odd number of inversions (FIG. 4 shows three inverters 38). If the input clock signal 37 is at 0, the signal 39 assumes the value 1 and the output signal 41 of the XOR gate 40 assumes the value 1. If the input clock signal 37 changes from 0 to 1, the new value 1 is immediately available at the first input of the XOR gate 40. The signal 39 only

changes to the new value 0 after a certain time delay that is determined by the gate delay of the three inverters 38. During a period that is characteristic of the gate delay, the output signal 41 is, therefore, at 0 and then it assumes the value 1.

Appellants explained on page 22 of the specification, line 12, that, the duration of the pulses in the output signal 41 represents a measure of the switching speed of the transistors of the substrate. The measurement makes it possible to detect the effect of process spreads on the transistor switching speed directly on the chip and to take it into consideration during the clock generation. Instead of the XOR gate, an XNOR gate can also be used for determining the switching speed of the transistors.

Appellants further explained on page 22 of the specification, line 21, that, FIG. 5A illustrates the variation with time of the input clock signal 37 and of the output signal 41 of the XOR gate 40. When the input clock signal 37 changes from 1 to 0, a falling signal edge 42 is obtained that triggers a pulse 43 with a pulse width t_D in the output signal 41. During the pulse period t_D, the output signal 41 assumes the value 0.

Appellants outlined on page 23 of the specification, line 2, that, when the input clock signal 37 changes from 0 to 1, a rising signal edge 44 is obtained that also triggers a pulse 45 of length t_D. The pulses 43, 45 shown in FIG. 5A are short and the corresponding values of t_D are low. Accordingly, the inverters 38 only produce a slight signal delay, which allows a high switching speed of the transistors and a short transient response of the operational amplifiers to be inferred.

Appellants stated on page 23 of the specification, line 11, that the pulse signal 41 is supplied to the programmable clock generator that digitizes the period of the pulses 43, 45 and uses them for calculating the switching clock configuration. For the case of a short pulse duration t_D shown in FIG. 5A, the switching clock signals generated by the programmable clock generator, the even switching-clock signal 46, and the odd switching-clock signal 47 are shown in FIG. 5B. Because of the fast transient response of the operational amplifiers, only short on-phases 48, 49 are required.

Appellants mentioned on page 23 of the specification, line 21, that the switching clock phases 50, 51, in which both switching-clock signals 46 and 47 are in the off-phase, can be correspondingly extended. In the prior art clock

configuration shown in FIG. 2B, the common off-phases had the period δ. In the clock configuration shown in FIG. 5B, however, the duration of the common off-phases has been increased to $\delta + t_a$. The operational amplifiers are only switched on until the transient is finished. During the common off-phases, all operational amplifiers are inactive.

Appellants described on page 24 of the specification, line 16, that FIG. 6A shows the input clock signal 52 and the output signal 53 of the XOR gate 40 for the case of transistors switching slowly or for long gate delays. The falling signal edge 54 causes a pulse 55 of duration t_D in the output signal 53 and the rising signal edge 56 correspondingly causes a pulse 57 of duration t_D. In the example shown in FIG. 6A, the transistors only have a low switching speed. The inverters 38, therefore, delay the signal considerably and the delay leads to a long pulse duration t_D, making it possible to infer a slow transient response of the operational amplifiers.

As set forth on page 24 of the specification, line 16, FIG. 6B shows the variation with time of the associated switching-clock signals, the even switching-clock signal 58 and the odd switching-clock signal 59. Because of the slow transient response of the operational amplifiers, the on-phases 60, 61 of the two switching-clock signals must be selected to be

long. Accordingly, the common off-phase 62 of the switching-clock signals must be reduced to the minimum period δ. Accordingly, t_a is set to be = 0.

As mentioned on page 25 of the specification, line 1, the programmable clock generator maps the pulse duration t_D onto the duration of the common off-phase $\delta + t_a$, a small value of t_D being mapped onto a large value of $\delta + t_a$ and a large value of t_D being mapped onto a small value of t_a. As such, the switching clock configuration can be adapted to the switching speed of the transistors such that the power saving is at a maximum.

Appellants explained on page 25 of the specification, line 9, that FIG. 7 illustrates an embodiment of the circuit 33 for determining the transistor switching speed that selectively detects the switching characteristic of n-type MOSFETs. The use of such a circuit is recommended if the transient response of the operational amplifiers used is mainly determined by the characteristics of the transistors of the n-type. The circuit includes the p-type MOSFETs 65, 66, 67 and the n-type MOSFETs 68, 69, 70, 71, 72, 73. The current through the FETs depends on the width/length ratio (W/L) of the respective FET. In the example illustrated in FIG. 7, the p-type FETs 65, 66, 67 and the n-type FETs 68, 69, 70 have a large W/L. The n-type FETs

71, 72, 73, the W/L ratio of which is much lower than that of the other devices, therefore, have a current-limiting effect.

Appellants further explained on page 25 of the specification, line 23, that, when the input signal 63 changes to VSS, the p-type FET 65 is gated on. The gate of the n-type MOSFET 69 is then at VDD and, if VBIAS has been suitably selected, the n-type FET 72 is also conducting. The potential VSS can then be switched through to the gate of the p-type FET 67. The p-type FET 67 places an input of the XOR gate 64 at VDD. Because of the low value of W/L in the case of the n-type FET 72, in comparison with the W/L values of the FETs 65, 67, 69, the total delay is essentially determined by the n-type FET 72. When the input signal 63 changes to VDD, in contrast, the total delay essentially depends on the switching speed of the n-type FETs 71 and 73. In every case, the total delay is, therefore, mainly determined by the n-type FETs having a small W/L.

Appellants outlined on page 26 of the specification, line 12, that FIG. 8 illustrates a method of how the clock configuration according to the invention can be generated externally by a squarewave generator and a divider circuit. The squarewave generator supplies a squarewave signal 74 having the frequency (2 f_{clk}). From the squarewave signal 74,

the even switching-clock signal 75 and the odd switching-clock signal 76, which each have a period of $\frac{1}{f_{clk}}$, are derived by a divider circuit.

Appellants stated on page 26 of the specification, line 20, that the duration of the common off-phase in which both switching-clock signals are equal to 0 can be adjusted by varying the duty ratio of the squarewave signal. The duty ratio of the squarewave signal 74 is 1/2 whereas the duty ratio of the squarewave signal 77 is 1/4. The squarewave signal 78 has a duty ratio of 3/4. The values of $\delta + t_a$ that belong to the individual duty ratios can be seen in the clock configuration illustrated in FIG. 8. The greater the selected duty ratio, the shorter the duration of the common off-phase $\delta + t_a$. Conversely, a small duty ratio produces a distinct extension of the common off-phase. The external circuit shown in FIG. 8 makes it possible to find out the magnitude of the spread of the transient response with a certain switched op-amp circuit and whether or not there is still potential for saving power.

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 17 - 21 and 24 are anticipated by U. S. Patent No. 5,745,002 to Bachirotto et al., under 35 U.S.C. §102(b).

2. Whether or not claims 1 - 5, 7, 9 - 12, 15 - 16 and 28 - 31 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al., 4,551,638 to Varadarajan and 6,392,466 to Fletcher, under 35 U.S.C. §103.

3. Whether or not claim 8 is obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al. and 6,392,466 to Fletcher, and further in view of U. S. Patent No. 5,097,208 to Chiang, under 35 U.S.C. §103.

4. Whether or not claims 13 - 14 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al. and 6,392,466 to Fletcher, and further in view of U. S. Patent No. 4,951,303 to Larson, under 35 U.S.C. §103.

5. Whether or not claims 22 - 23 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al., under 35 U.S.C. §103.

6. Whether or not claims 25 - 27 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent No. 4,951,303 to Larson, under 35 U.S.C. §103.

Argument:

Claims 1, 15, 16 and 17 are independent. Claims 2 - 5 and 7 - 14 depend, ultimately, on claim 1, while claims 18 - 29 depend, ultimately, from claim 17, claim 30 depends from claim 15 and claim 31 depends from claim 16. The patentability of claims 1, 7, 15, 16, 17, 21, 28, 29, 30 and 31 are all separately argued.

I. Whether or not claims 17 - 21 and 24 are anticipated by U. S. Patent No. 5,745,002 to Bachirotto et al., under 35 U.S.C. §102(b).

A. Claim 17 is not anticipated by the Bachirotto et al., reference

Claim 17 of the instant application relates to a method for clocking successive operational amplifier stages constructed in switched op-amp technology. Among other limitations, Appellants' claim 17 requires:

> "generating at least two non-overlapping switching-clock signals;
>
> switching a first operational amplifier on and off with a first signal of the two switching-clock signals;

switching a second operational amplifier on and off with a second signal of the switching-clock signals;"

As is explained in the instant application, page 17, line 6, - page 19, line 5, in connection with Figs. 1, 2A and 2B of the application, in the prior art, a first operational amplifier and a second operational amplifier are switched on and off with two non-overlapping switching-clock signals (27 and 30 of Fig. 2B of the instant application). These two non-overlapping switching-clock signals 27 and 30 of the prior art system of Fig. 2B are non-overlapping, **because there exists a period of delay "δ"** during which both of these signals 27 and 30 are off. The above-described method shows how the art, prior to Appellants' claimed invention, clocked successive operational amplifier stages constructed in switched op-amp technology. Fig. 2B of the instant application, depicting the prior art switching clock signals 27 and 30, is provided herebelow for convenience.

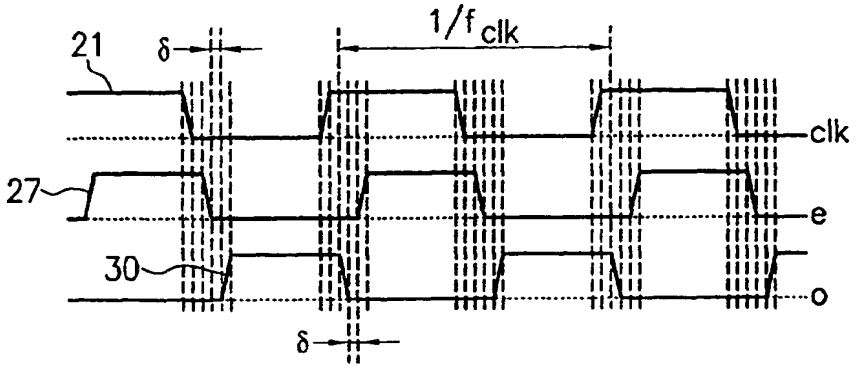


Fig.2B
PRIOR ART

However, Appellants' invention of claim 17 operates differently from the above-described prior art. More particularly, Appellants' claim 17, is distinguished from the above-described prior art because, Appellants' claim 17 further recites, among other limitations:

> "**varying switching-clock phases** of the first and second signals in which the operational amplifiers are switched off; and
>
> **providing a variable delay between the switching-clock phases** of the first and second signals during which the operational amplifiers are switched off." [emphasis added by Appellants]

Thus, the method according to claim 17 doesn't use a **fixed** common off-phase delay "δ", as does the prior art, but, rather, requires the use of a **variable** common off-phase delay. The **variability** of the common off-phase delay in Appellants' claim 17, provides for a power savings in switched op-amp technology **by optimizing the period of the common off-phase delay**.

Like the prior art described in the instant application, in connection with Figs. 1, 2A and 2B, United States Patent No. 5,745,002 to Baschirotto et al ("**BASCHIROTTO**") fails to teach or suggest, among other limitations of Appellants' claim 17: (1) **varying switching-clock phases** of the first and second signals in which the operational amplifiers are switched off;

and (2) **providing a variable delay between the switching-clock phases** of the first and second signals during which the operational amplifiers are switched off.

In the final Office Action of April 18, 2005 ("**final Office Action**"), it is stated on page 3, item 5.9, that the circuit configuration in **BASCHIROTTO** includes a phase-variance device. More particularly, item 5.9 of the **final Office Action**, alleges, with regard to **BASCHIROTTO:**

> "The circuit configuration comprising a phase-variance device [**Fig. 5; inherently, there is a phase-variance device**, in the broadest interpretation, to output the different phases] varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase [**col.8, ll. 1-5;** suitably delaying or varying the phases]." [emphasis added by Appellants]

Appellants respectfully disagree with the statement that **BASCHIROTTO** discloses a phase-variance device. Fig. 5 of **BASCHIROTTO**, cited in the **final Office Action** as allegedly showing a phase-variance device, shows the switching signals F1, $F1_a$, F2, $F2_a$. Fig. 5 of **BASCHIROTTO** is provided herebelow for convenience:

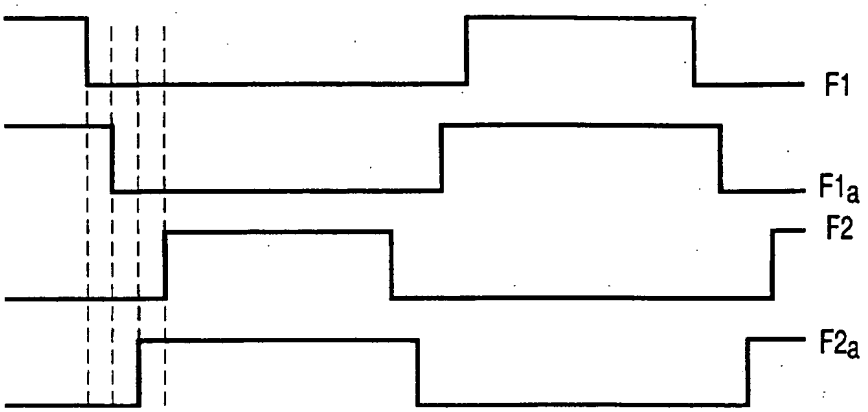


FIG. 5

In **BASCHIROTTO**, $F1_a$ is the power switching signal for switching the operational amplifier A1 and F2a is the power switching signal for switching the operational amplifier A2. As can be seen from Fig. 5 of **BASCHIROTTO**, the common off-phase delay is located between the second and the third dashed vertical lines shown in Fig. 5 (denoted as lines B and C in the Office action).

Thus, quite similar to the prior art, as depicted in Fig. 2B of the instant application, Fig. 5 of **BASCHIROTTO** shows **that there is a common off-phase of the switching signals F1a and F2a. Fig. 5 clearly does not disclose or suggest that this common off-phase is varied.** As such, Fig. 5, by itself, does not support the allegation made in item 5.9 of the **final Office Action** (i.e., that **BASCHIROTTO** discloses a phase-

variance device). Nor does col. 8 of **BASCHIROTTO**, lines 1 - 5 disclose **varying switching-clock phases**, as required by Appellants' claim 17. Rather, col. 8 of **BASCHIROTTO**, lines 1 - 5, cited in the **final Office Action** as allegedly disclosing **varying switching-clock phases**, merely states"

> "Of course this may be easily implemented by driving the switches with clock phase signals suitably delayed in respect to the homologous clock phase signals that turn on the operational amplifiers A1 and A2 and drive the switches S5 and S2'."

Appellants' respectfully disagree that the portions of **BASCHIROTTO** cited in the final **Office Action** disclose varying the phase of the common off-phase of signals $F1_a$ and $F2_a$, as required by Appellants' claim 17. The above quoted portion of **BASCHIROTTO** cited in the final **Office Action** merely states that clock phase signals of **BASCHIROTTO** may be "suitably delayed in respect to the homologous clock phase signals". Appellants respectfully disagree that implementing a suitable delay between signals is analogous **to providing a varying delay of these signals**. Obviously, the only reason which is conceivable for the Examiner's interpretation relies on the word "suitably". However, it is clear from the context of the preceding paragraph, column 7 of **BASCHIROTTO**, lines 62 - 67, that the chosen delay will be "suitable" in order to reduce the negative switching spikes produced by the injection of charge effected by the capacitor Cdc on the node N2 (column 7

of **BASCHIROTTO**, lines 51 - 53). Merely disclosing the implementation of a "suitable delay" (i.e. suitably large) **does not teach or suggest providing a variable delay between the phases, as required by Appellants' claim 17.**

Clearly, the analysis made in the **final Office Action** uses **impermissible hindsight reconstruction to recreate Appellants' invention of claim 17** by adding the concept of "varying" to the wordings "suitably delaying" in the **BASCHIROTTO** reference, where there is otherwise no motivation to do so.

Further, as explained in Appellants' response to the previous Office Action (the "**Response**"), in **BASCHIROTTO**, the signals indicated in col. 8, lines 1 - 5 as being "suitably delayed" **are not the signals $F1_a$ versus $F2_a$.** Rather, in the cited to portion of **BASCHIROTTO**, the wording "suitably delayed" **relates to the delay between the capacitor switching signals F1, F2 (i.e. switches S3, S4) and the op-amp power switch signals $F1_a$, $F2_A$ (i.e. switches S5, S2'), respectively.** In other words, referring to the illustration made on page 2 of the **final Office Action**, the delay **A-B** between the signals F1 (capacitor discharge) and $F1_a$ (operational amplifier A1) and the delay **C-D** between the signal F2 (capacitor discharge) and the signal $F2_a$ (second operational amplifier power switch) are what is being discussed in col. 8, lines 1 - 5 of **BASCHIROTTO**, **and not the**

delay between the signals $F1_a$ and $F2_a$.

In view of the foregoing, Appellants believe thay have shown how **BASCHIROTTO** fails to teach or suggest **varying a variable delay between two non-overlapping switching-clock signals switching a first and a second operational amplifier on and off**, as required by Appellants' claim 17. As such, Appellants' believe that claim 17 is patentable over the **BASCHIROTTO** reference.

B. Claims 18 - 21 and 24 are not anticipated by the Bachirotto et al., reference

Appellants' claims 18 - 21 and 24 all depend, ultimately, from Appellants' independent claim 17. As set forth in Section A, above, claim 17 is not anticipated by **BACHIROTTO**. As such, Appellants' claims 18 - 20 and 24, which contain all of the limitations of Appellants' claim 17, as well as other limitations, are additionally not anticipated by the **BACHIROTTO** reference.

II. Whether or not claims 1 - 5, 7, 9 - 12, 15 - 16 and 28 - 31 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al., 4,551,638 to Varadarajan and 6,392,466 to Fletcher, under 35 U.S.C. §103.

A. Appellants' Independent Claims 1, 15 and 16 are Patentable Over the Cited References.

Appellants' independent claims 1, 15 and 16 all recite to a circuit configuration containing, among other limitations:

> "at least one switchable operational amplifier having an input and an output and transistors having a switching speed;
>
> at least one sampling capacitor connected to said input;
>
> at least one integrating capacitor connected to said input and to said output;"

Further, each of claims 1, 15 and 16 recite, among other limitations, a particularly claimed clock generator (claims 1 and 15) or clock generator means (claim 16) "producing a first and a second switching signal each having switching-clock phases including an on-phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping". The clock generator of claims 1, 15 and 16 additionally:

> "**controlling charging of said sampling capacitor with said first switching-clock signal** and **switching said operational amplifier on and off with said second switching-clock signal.**" [emphasis added by Appellants]

Further, the circuit configuration of Appellants' claims 1, 15 and 16 recites, among other limitations, includes:

> "a **detector for detecting the switching speed of said transistors** .."

and, claims 1 and 15 further require, among other limitations:

> "a **phase-variance device** . . ., said phase-variance device being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing that duration when said switching speed is low." [emphasis added by Appellants]

Appellants claim 16, similarly recites:

> "a **phase-variance means** . . ., said phase-variance means being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing that duration when said switching speed is low." [emphasis added by Appellants]

As correctly stated in item 19 of the **final Office Action**:

> "Baschirotto **did not discuss a detector** for detecting the switching speed of the transistors and **did not discuss the details of the phase-variance device**". [emphasis added by Appellants]

As stated above in connection with Section I(A), Appellants' believe that **BASCHIROTTO** not only fails to discuss the details of **a phase-variance device**, but also completely fails to teach or suggest phase-varying, at all.

Item 19 of the **final Office Action** goes on to allege, however, that claims 1, 15 and 16 are rendered obvious by **BASCHIROTTO** in view of U. S. Patent No. 5,723,996 to Saito et al ("**SAITO**"), U. S. Patent No. 4,551,638 to Varadarajan ("**VARADARAJAN**") and U. S. Patent No. 6,392,466 to Fletcher ("**FLETCHER**").

Appellants' respectfully disagree.

FLETCHER relates to a controllable pulse clock delay arrangement to control functional race margins in a logic data path. To this end, a logic block 470b (Fig. 9 of **FLETCHER**) is connected with a controllable pulse clock delay 480b controlling the operation mode of the associated functional block 470b. More specifically, the pulse clock delay 480b (also shown in Figs. 6 and 7 of **FLETCHER** and denoted therein by reference sign 100) produces stretched or shortened delays in order to reducing processing delays and/or power consumption of the logical data path (see **FLETCHER**, col. 8, line 61; col. 8, lines 45 - 48; and col. 21, lines 29 - 43).

A person skilled in the art would in no way be motivated to apply Fletcher's teaching to generate a delayed output clock signal based on an input clock signal to the switched op-amp circuit shown in Fig. 4 of **BASCHIROTTO**. First, as already

mentioned, **BASCHIROTTO** does not teach, among other limitations, **providing a variable delay** between two clock signals, and therefore, there would be no motivation for a person skilled in the art to look for any information how to generate such a **variable delay**.

Second, the disclosure in **FLETCHER** to generate a delayed output clock signal based on an input clock signal neither relates to **the common off-phase of two clock signals controlling the charging of a sampling capacitor**, nor to the **powering of an operational amplifier**. As such, it does not follow that, a person skilled in the art would, without any suggestions from the prior art, use the phase delayed clock signal 460b of **FLETCHER**, controlling the operation of the logic block 470b, to control the switching signals in a switched op-amp configuration, as in **BASCHIROTTO**.

Further, the **SAITO** reference, cited in the **final Office Action**, discloseS a detector 121 for measuring the operating speed of transistors. In **SAITO**, when the operating speed of the transistors is low, the clock selecting circuit 122 selects a low speed clock CK1. Then, in **SAITO**, when the operating speed is high, a high-speed clock CK2 is selected. See **SAITO**, col. 5, lines 46 to 54) .

In the **final Office Action**, it is alleged that a person skilled in the art would combine **BASCHIROTTO** and **SAITO**, to use the detector disclosed in **SAITO** in the circuit configuration of **BASCHIROTTO**. Appellants' respectfully disagree.

First, as **BASCHIROTTO** fails to teach or suggest any phase-variance device, no phases are varied and therefore, no detector is needed to control any phase-variation. However, even if the allegation in the **final Office Action** is adopted, arguendo, **BACHIROTTO** in combination with **SAITO** would teach a person of skill in the art **to vary <u>the clock rate</u>** of an electronic circuit, dependent upon the measured switching speed of the transistors, but the combination would not teach a person skilled in the art to not **to vary <u>the delay</u>**, as required by Appellants' claims 1, 15 and 16.

Thus, applying the teaching of **SAITO** to what is allegedly disclosed in **BASCHIROTTO** would merely propose to vary the clock rate (i.e. the common period length of the signals F1, $F1_a$, F2, $F2_a$) of the switched op-amp circuit illustrated in Fig. 4 of **BASCHIROTTO** . However, the combination of **BASCHIROTTO** and **SAITO** would definitely not teach, suggest or motivate **varying <u>a duration of the switching clock phases depending on transistor speed</u>**, according to the present invention.

Further, the detector 121 disclosed of **SAITO** could not be combined with the controllable phase-delay element disclosed in **FLETCHER**. Fletcher discloses to vary the delayed output clock signal in dependence of the intended operation mode of the associated functional block, **but does not give any indication of varying the delay as a function of any detected parameters like the switching speed of transistors**. Therefore, there is no teaching, suggestion or motivation, to control the controllable phase-delay element of **FLETCHER** with the detector of **SAITO**.

Further, claims 1, 15 and 16 require, among other limitations, that the phase-variance device **enlarges the common off-phase duration when the switching speed is high** and **reduces the common off-phase duration when said switching speed is low**. It is alleged in item 19 of the **final Office Action** that the above feature of Appellants' claims can be found in **VARADARAJAN**. The **VARADARAJAN** reference discloses an ECL OR/NOR gate with a switched load current source. More particularly, in **VARADARAJAN** a single current source 30 is switched between two load current source transistors 10 and 11. See **VARADARAJAN**, col. 3, lines 42 - 45; and col. 4, lines 14 - 16). As described in col. 6 of **VARADARAJAN**, lines 26 - 52, the additional delay introduced by the switchable power

source is the delay between the level rise on node c (Fig. 5A of **VARADARAJAN**) and the output transitions experienced at the OR output 18 and the NOR output 19 as shown in Figs. 5B and 5C of **VARADARAJAN**.

Item 8.1 of the **final Office Action** alleges that **VARADARAJAN** discloses:

> "a circuit configuration comprising a device [ECL gate] for enlarging a duration [from activation of driving signal which switches the transistor to onset of delay] when a switching speed is high and reducing the duration when the switching speed is low".

Appellants respectfully disagree with the allegation made in item 8.1 of the **final Office Action**. **VARADARAJAN** simply states in the passage cited in the **final Office Action, that any possible delay added by the switching transistor (used for switching the single current source between the two load current source transistors) should be as short as possible and that any possible delay should be more than compensated by the reduction in power achieved by providing only a single (switched) current source (and not two current sources).**

In view of the foregoing, it can be seen that the **BASCHIROTTO SAITO, VARADARAJAN and FLETCHER** references cited in the final Office Action against Applicants' independent claims 1, 15 and 16, neither teach, nor suggest, Appellants' claimed invention,

whether taken alone, or in combination.

B. Appellants' Dependent Claim 28 is Patentable Over the Cited References.

Appellants' claim 28 depends from independent claim 17, and as such is believed to be patentable **BASCHIROTTO** for the same reason as disclosed in Section I(A) above. Further, claim 28 recites, among other limitations:

> "varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low."

The added limitations of Appellants' claim 28 are discussed in detain in section II(A) above, and for the same reasons given therein, it can be seen that the combination of **BASCHIROTTO, SAITO**, **VARADARAJAN** and **FLETCHER** fails to teach or suggest all of the limitations of Appellants' dependent claim 28..

C. Appellants' Dependent Claim 7, 29, 30 and 31 are Patentable Over the Cited References.

Claims 7, 29, 30 and 31 recite, among other limitations, that the claimed **detector separately detects the switching speed of n-type channel FETs and p-type channel FETs**. This claim feature is advantageous because n-type channel FETs and p-type

channel FETs may differ considerably with regard to their switching speeds. See page 7 of the instant application, lines 22 - 26.

The **SAITO** reference discloses that the operating speed-measuring circuit (121 of **SAITO**) measures the switching speed of transistors constituting the processor. See **SAITO**, col. 5, lines 40 - 42. **SAITO**. does not disclose distinguishing between n- and p-type channel transistors when detecting the switching speed of transistors. As such, **SAITO** fails to teach or suggest all the limitations of Appellants' claims 7, 29, 30, 31.

Rather, it is alleged in item 24 of the **final Office Action** that:

> "24.1. Bashirotto discloses the circuit configuration wherein the transistors include at least one of n-channel FETs and p-channel FETs [fig. 10] and the transistors each have a respective switching speed **[inherently, each transistor will have a switching speed in the broadest interpretation]**.
>
> 24.2. Saito discloses the detector detects the switching speed of the transistors [col. 5, ll. 35-57; **detector detects switching speed of at least one of the kind of transistors**]." [emphasis added by Appellants]

Appellants respectfully disagree with the logic alleged in paragraph 24 of the **final Office Action.** **SAITO** merely

discloses the operating speed measuring detector 121 as a block in Fig. 5, **without providing any detailed circuitry.** Therefore, a person of skill in the art is not given any information on how the operating speed measurement detector 121 of **SAITO** is implemented. In the Office Action, it is alleged that "**inherently, each transistor will have a switching speed in the broadest interpretation**", and as such, it is implied, a detector will detect each switching speed of each transistor. Thus, it is alleged that the detector of **SAITO separately detects the switching speed of n-type channel FETs and p-type channel FETs.** The conclusion of item 24 of the **final Office Action** is completely unsupported. Just because **SAITO** detects transistor speeds **and** because each transistor has a speed, **does not teach or suggest Appellants' particularly recited limitation of separately detects the switching speed of n-type channel transistors and of p-type channel transistors** of claims 7, 29, 30 and 31. **SAITO** provides no indication, no teaching, no suggestion and no motivation to a person skilled in the art to contemplate **a separate detection of the switching speed of n-type channel FETs and p-type channel FETs**. Nor do any of the other references (**BASCHIROTTO, VARADARAJAN** and **FLETCHER**) cited in the rejection of claims 7, 29, 30 and 31. In view of the foregoing, claims 7, 29, 30 and 31 are believed to be patentable over the cited references, alone or in combination.

D. Appellants' Dependent Claim 2 - 5 and 9 - 12 are Patentable Over the Cited References.

Appellants' claims 2 - 5 and 9 - 12 all depend, ultimately, from Appellants' independent claim 1. As set forth in Section A, above, claim 1 is believed to be unobvious over the combination of **BASCHIROTTO, SAITO, VARADARAJAN** and **FLETCHER**. As such, Appellants' claims 2 - 5 and 9 - 12, which contain all of the limitations of Appellants' claim 1, as well as other limitations, are additionally believed to be unobvious over the combination of **BASCHIROTTO, SAITO, VARADARAJAN** and **FLETCHER**.

III. Whether or not claim 8 is obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al. and 6,392,466 to Fletcher, and further in view of U. S. Patent No. 5,097,208 to Chiang, under 35 U.S.C. §103.

Appellants' claim 8 depends from Appellants' independent claim 1. As set forth in Section II(A), above, claim 1 is believed to be unobvious over the combination of **BASCHIROTTO, SAITO, VARADARAJAN** and **FLETCHER**. In the **final Office Action, CHIANG** is further combined with **BASCHIROTTO, SAITO** and **FLETCHER**. However, the **CHIANG** reference does not overcome the above described deficiencies/failures in the teachings of **BASCHIROTTO, SAITO, FLETCHER** and/or **VARADARAJAN**, with regard

to Appellants' claim 1. As such, Appellants' claim 8, which contain all of the limitations of Appellants' claim 1, as well as other limitations, is additionally believed to be unobvious over the combination of **BASCHIROTTO, SAITO, VARADARAJAN, FLETCHER** and **CHIANG**.

IV. Whether or not claims 13 - 14 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al. and 6,392,466 to Fletcher, and further in view of U. S. Patent No. 4,951,303 to Larson, under 35 U.S.C. §103.

Appellants' claims 13 - 14 depend, ultimately, from Appellants' independent claim 1. As set forth in Section II(A), above, claim 1 is believed to be unobvious over the combination of **BASCHIROTTO, SAITO, VARADARAJAN** and **FLETCHER**. In the **final Office Action**, **LARSON** is further combined with **BASCHIROTTO, SAITO** and **FLETCHER**. However, the **LARSON** reference does not overcome the above described deficiencies/failures in the teachings of **BASCHIROTTO, SAITO, FLETCHER** and/or **VARADARAJAN**, with regard to Appellants' claim 1. As such, Appellants' claims 13 and 14, which contain all of the limitations of Appellants' claim 1, as well as other limitations, is additionally believed to be unobvious over the combination of **BASCHIROTTO, SAITO, VARADARAJAN, FLETCHER** and **LARSON**.

V. Whether or not claims 22 - 23 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent Nos. 5, 723,998 to Saito et al., under 35 U.S.C. §103.

A. Claims 22 and 23 are obvious over BASCHIROTTO in view of SAITO

Claim 21 of the instant application depends from independent claim 17 and, for the reasons stated above in Section A, claim 21 is not anticipated by the **BASCHIROTTO** reference. Further, Appellants' dependent claim 21 additionally recites, among other limitations,

> "**varying a duration of the switching-clock phases** in which the operational amplifiers are switched off **dependent on a switching speed of transistors** of the operational amplifiers." [emphasis added by Applicants]

Appellants' dependent claims 22 and 23, depending from claims 17 and 21, respectively, further recite, among other limitations:

> "separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs."

As already discussed above, in section II(A), **SAITO**. discloses the measurement of the switching speed of transistors. However, rather than varying a common off-phase duration of two switched operational amplifiers **SAITO**, merely discloses **controlling the clock rate of the circuit**, e.g. to accelerate

or decelerate the entire data processing in the processor. Therefore, claim 21 is not rendered obvious by **BASCHIROTTO** in view of **SAITO**, as alleged in item 43 of the **final Office Action**. Further, as set forth above in Section II(C), both **BASCHIROTTO** and **SAITO** fail to teach or suggest **separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs**, as required by Applicants' claims 22 and 23.

As such, it is believed that claims 22 and 23 are patentable over the combination of **BASCHIROTTO** and **SAITO**.

VI. Whether or not claims 25 - 27 are obvious over U. S. Patent No. 5,745,002 to Bachirotto et al. in view of U. S. Patent No. 4,951,303 to Larson, under 35 U.S.C. §103.

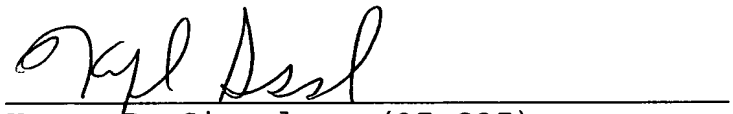
Appellants' claims 25 - 27 depend, ultimately, from Appellants' independent claim 17. As set forth in Section I(A), above, claim 17 is believed to not be anticipated by **BASCHIROTTO**. In the **final Office Action**, **LARSON** is further combined with **BASCHIROTTO** to allegedly render claims 25 - 27 obvious. However, the **LARSON** reference does not overcome the above described deficiencies/failures in the teachings of **BASCHIROTTO** with regard to Appellants' claim 17. As such, Appellants' claims 25 - 27, which contain all of the limitations of Appellants' claim 17, as well as other

limitations, are additionally believed to be unobvious over the combination of **BASCHIROTTO** and **LARSON**.

VII. Conclusion.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,



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Claims Appendix:

1. A circuit configuration in switched op-amp technology, comprising:

at least one switchable operational amplifier having an input and an output and transistors having a switching speed;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a detector for detecting the switching speed of said transistors, said detector being connected to said operational amplifier;

a clock generator producing a first and a second switching signal each having switching-clock phases including an on-phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping;

said clock generator controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance device connected to said clock generator, said phase-variance device being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

2. The circuit configuration according to claim 1, wherein said phase-variance device is configured to vary each of said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

3. The circuit configuration according to claim 1, wherein said phase-variance device is configured to vary each second one of said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

4. The circuit configuration according to claim 1, wherein:

said operational amplifier has a transient response; and

said phase-variance device is configured to vary a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said transient response of said operational amplifier.

5. The circuit configuration according to claim 1, wherein:

said operational amplifier has transistors having a switching speed; and

said phase-variance device is configured to vary a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors.

7. The circuit configuration according to claim 1, wherein:

said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.

8. The circuit configuration according to claim 1, including an inverter chain, said detector having one of:

an XOR gate with XOR inputs, one of said XOR inputs receiving an undelayed edge signal, and another of said XOR inputs receiving the edge signal delayed through said inverter chain; and

an XNOR gate with XNOR inputs, one of said XNOR inputs receiving the edge signal and another of said XNOR inputs receiving the edge signal delayed through said inverter chain.

9. The circuit configuration according to claim 1, wherein said detector generates detector pulses having a duration characterizing said switching speed of said transistors.

10. The circuit configuration according to claim 9, wherein said phase-variance device is configured to adjust a duration of said switching-clock phases in which said first and second

switching-clock signals are in said off-phase dependent upon a duration of said detector pulses.

11. The circuit configuration according to claim 1, wherein said phase-variance device is configured to adjust a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase in a given number of predetermined steps.

12. The circuit configuration according to claim 1, wherein said clock generator and said phase-variance device are embodied as a programmable clock generator.

13. The circuit configuration according to claim 1, wherein said clock generator and said phase-variance device are embodied as:

an external squarewave generator producing a squarewave signal; and

a divider circuit connected to said squarewave generator, said divider circuit generating said at least two switching-clock signals from said squarewave signal.

14. The circuit configuration according to claim 13, wherein:

said squarewave signal has a duty ratio; and

adjustment of said duty ratio varies said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

15. A circuit configuration in fully differential circuit technology, comprising:

at least one switchable operational amplifier having an input and an output and transistors having a switching speed;
at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a detector for detecting the switching speed of said transistors, said detector being connected to said operational amplifier;

a clock generator producing a first and a second switching signal each having switching-clock phases including an on-

phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping;

said clock generator controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance device connected to said clock generator, said phase-variance device being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

16. A circuit configuration in switched op-amp technology, comprising:

at least one switchable operational amplifier having an input and an output and transistors having a switching speed;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a detector for detecting the switching speed of said transistors, said detector being connected to said operational amplifier;

clock generator means for generating a first and a second switching signal each having an on-phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping;

said clock generator means controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

phase-variance means for varying switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance means connected to said clock generator means, said phase-variance means being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals

are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

17. A method for clocking successive operational amplifier stages constructed in switched op-amp technology, which comprises:

generating at least two non-overlapping switching-clock signals;

switching a first operational amplifier on and off with a first signal of the two switching-clock signals;

switching a second operational amplifier on and off with a second signal of the switching-clock signals;

varying switching-clock phases of the first and second signals in which the operational amplifiers are switched off; and

providing a variable delay between the switching-clock phases of the first and second signals during which the operational amplifiers are switched off.

18. The method according to claim 17, which further comprises varying each of the switching-clock phases in which the operational amplifiers are switched off.

19. The method according to claim 17, which further comprises varying each second one of the switching-clock phases in which the operational amplifiers are switched off.

20. The method according to claim 17, which further comprises varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a transient response of the operational amplifiers.

21. The method according to claim 17, which further comprises varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a switching speed of transistors of the operational amplifiers.

22. The method according to claim 17, which further comprises separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs.

23. The method according to claim 21, which further comprises separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs.

24. The method according to claim 17, which further comprises adjusting a duration of the switching-clock phases in which the operational amplifiers are switched off in a number of predetermined steps.

25. The method according to claim 17, which further comprises generating the at least two non-overlapping switching-clock signals with a programmable clock generator.

26. The method according to claim 17, which further comprises generating the at least two non-overlapping switching-clock signals with an external squarewave generator and a divider circuit.

27. The method according to claim 26, which further comprises varying the switching-clock phases in which the operational amplifiers are switched off by adjusting a duty ratio of a squarewave signal from the squarewave generator.

28. The method according to claim 17, which further comprises varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

29. The method according to claim 17, which further comprises:

providing said transistors with at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each having a respective switching speed; and

separately detecting said switching speed of said n-channel FETs and said p-channel FETs.

30. The circuit configuration according to claim 15, wherein:

said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.

31. The circuit configuration according to claim 16, wherein:
said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.

Evidence Appendix:

No evidence pursuant to && 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

Since there are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, no copies of decision rendered by a court or the Board are available.